Evaluating TMR Techniques in the Presence of Single Event Upsets

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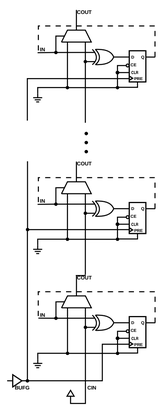
1 Introduction

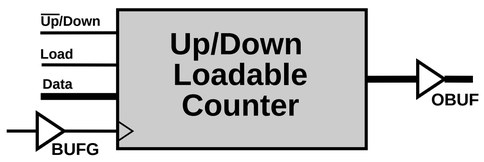
Triple modular redundancy (TMR) is a technique commonly used to provide design hardening. The purpose of this paper is to investigate the effectiveness and cost of different TMR styles in order to improve the reliability of SRAM-based FPGA designs in the face of single event configuration upsets. To measure the effectiveness of TMR, we determine the number of sensitive configuration bits in designs hardened with each TMR style. A sensitive bit bit is defined as a bit which, when toggled, changes the behaviour of the circuit. A simulator developed at BYU [1] is used to exhaustively test the sensitivity of every configuration bit of a Virtex V1000 FPGA. This simulator was developed in order to evaluate how sensitive a given design is to configuration SEUs. With the aid of this simulator, we can show that certain TMR techniques will lead to zero configuration upsets. Specifically, we get zero SEU failures when feedback TMR is used and the clocks are triplicated. Specially mapped feedback TMR[2] with triplicated clocks also results in zero SEU failures.

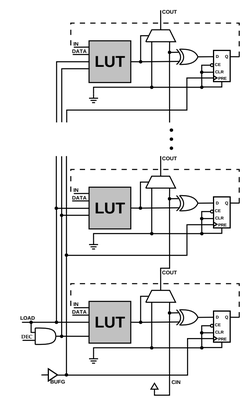
2 Baseline Designs

8-Bit Incrementer



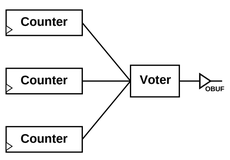
8-Bit Up/Down Loadable Counter





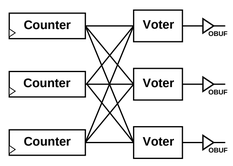
3 TMR Techniques

1 Voter TMR



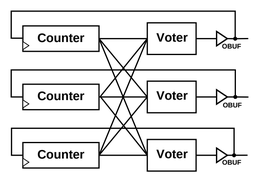
- Single point of failure in the voter
- Useful only when the voter size small relative to the rest of the circuit

3 Voter TMR



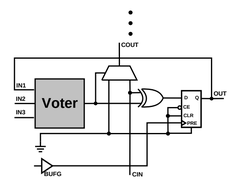
- Reliability greatly increases
- More LUTs required for additional voters

Feedback TMR



- Prevents synchronization errors
- Improved reliability
- Operates at slower speed

Mapped Feedback



- Voter merged into same LUT as counter
- Reduced number of LUTs required
- Only possible with incrementer

Design (single clock)	Simple Incrementer LUTs	Failures	Speed (MHz)	Up/Down Loadable Counter LUTs	Failures	Speed (MHz)
No Redundancy	8	446	220	10	463	220
1 Voter	35 (∼4x)	410	217 (99%)	41 (∼4x)	484	217 (99%)
3 Voters	51 (∼6x)	89	199 (91%)	57 (∼6x)	36	213 (97%)
Feedback	51 (∼6x)	14	160 (73%)	57 (∼6x)	15	157 (72%)
Map Feedback	27 (∼3x)	15	194 (88%)	N/A		

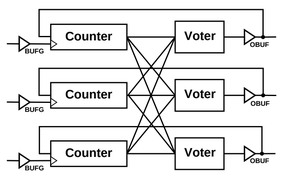
Table 1: Evaluation of TMR on 8-bit Counters

4 Architectural Techniques for TMR

Triplicated Clocks

- Single point of failure in clock domain
- Error free operation requires three clocks
- Feedback TMR and 3 clocks provides bulletproof designs

Bulletproof Design



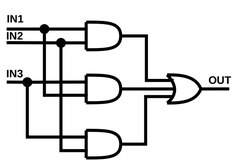
Design	Simple Incrementer Failures	Speed (MHz)	Up/Down Loadable Counter Failures	Speed (MHz)
3 Voters	99	201 (91%)	37	218 (99%)
Feedback	**0**	167 (76%)	**0**	158 (72%)
Map Feedback	**0**	204 (93%)	N/A	

Table 2: Evaluation of Triplicated clocks and TMR on 8-bit Counters

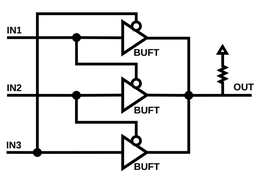
TBUF vs. LUT Voter

- 1 LUT required for each bit of LUT voter
- No LUTs required for TBUF voter
- 3 TBUFs required for each bit of TBUF voter
- TBUF voter runs slower than LUT voter

LUT Voter



TBUF Voter



Design	Simple Incrementer LUTs	Failures	Speed (MHz)	Up/Down Loadable Counter LUTs	Failures	Speed (MHz)
1 Voter	27 (∼3x)	293	219 (100%)	33 (∼3x)	425	212 (96%)
3 Voters	27 (∼3x)	30	219 (100%)	33 (∼3x)	32	213 (97%)
3 Voters, 3 Clk	27 (∼3x)	46	219 (100%)	33 (∼3x)	40	215 (98%)
Feedback	27 (∼3x)	19	106 (48%)	33 (∼3x)	14	102 (46%)
Feedback, 3 Clk	27 (∼3x)	**0**	123 (56%)	33 (∼3x)	**0**	117 (53%)
Map Feedback	27 (∼3x)	19	105 (48%)	N/A		
Map Feedback, 3 Clk	27 (∼3x)	**0**	123 (56%)			

Table 3: Evaluation of TBUF Voters with TMR on 8-bit Counters

5 Conclusion

- It is possible to completely eliminate SEU design failures for these designs i.e. **ZERO** failures
- TMR requires significant resources and reduces design speed

References

[1] Eric Johnson, Michael J. Wirthlin, and Michael Caffrey. Single-event upset simulation on an FPGA. In Toomas P. Plaks and Peter M. Athanas, editors, *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pages 68–73. CSREA Press, June 2002.

[2] Carl Carmichael. Triple module redundancy design techniques for Virtex FPGAs. Technical report, Xilinx Corporation, November 1, 2001. XAPP197 (v1.0).